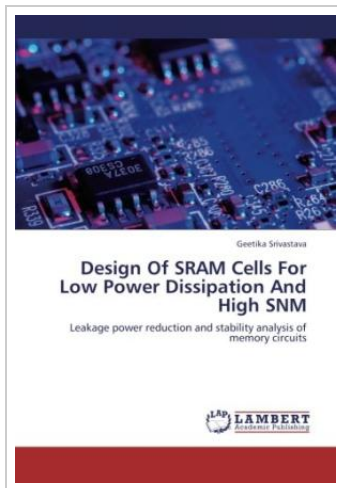




Design Of SRAM Cells For Low Power Dissipation And High SNM

By Srivastava, Geetika

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Leakage power reduction and stability analysis of memory circuits | During past few decades CMOS IC technologies have been aggressively scaled down to nanometer regime. Due to verity of demands of different circuit applications, integrated memories especially SRAM cell layout has been facing significant improvement. So in depth knowledge and detail analysis about the stability of the SRAM cells and the impact of physical parameters variation is a must in modern CMOS designs. As these high density circuits consume an excessive amount of power and generate an increased amount of heat they are more susceptible to run time failures and present serious reliability problems. SRAM arrays consume a large portion of the chip area in today s embedded system hence it seems very interesting as well as important to investigate this particular component. Circuit designers are realizing the importance of limiting power consumption and improving energy efficiency at all levels of design. Reducing the power dissipation in memories can significantly improve the system power-efficiency, performance, reliability, and overall costs. In this book various SRAM architectures with different leakage power reduction schemes have been investigated in Deep Submicron region. | Format: Paperback |...



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